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DESIGN AND IMPLEMENTATION OF HIGH RELIABLE 6T SRAM CELL

V.Vivekanand*, P.Aditya, P.Pavan Kumar

* Electronics and Communication Engineering Dept. GOKUL College of Engineering Vizianagaram, India.

Electronics and Communication Engineering Dept. GOKUL College of Engineering Vizianagaram, India.

ABSTRACT

This paper describes a design and implementation of a high reliable 6t SRAM cell with write and read operations. Low-power Random Access Memory (RAM) has seen a remarkable and rapid progress in power reduction. Many circuit techniques for active and standby power reduction in static and dynamic RAMS have been devised but Static random access memory (SRAM) is a critical part of most VLSI system-on-chip (SOC) applications. Conventional SRAM bit cell design consists of 6 transistors. This paper presents a new static random access memory (SRAM) cell with separate write and read circuits. The elementary cell structure of proposed SRAM cell consists of two high load resistors which are constructed of PMOS, and NMOS switch which is necessary to restrict short circuit current.

KEYWORDS: NBLV(NEGATIVE BIT LINE VOLTAGE),WL(WORD LINE) ,BL(BIT LINE) ,BLBAR.

INTRODUCTION

CMOS scaling for the past four decades has offered improved performance. However, as technology scaled down, standby power consumption increases exponentially with the decrease of threshold voltage of MOSFET devices. SRAM, which is one of the main building blocks in digital circuits, occupies about 90% of the area of a SOC in 2013. SRAM is also one of the important sources of static power consumption. Therefore, it is important to design new high performance, small area, and low power SRAM using novel devices.

CONVENTIONAL 6T SRAM CELL DESIGN

Access transistors enable access to the cell during read and write operations and provide cell isolation during the not-accessed state. an sram cell is designed to provide non-destructive read access, write capability and data storage (or data retention) for as long as cell is powered and it discusses about the design and analysis of two different sram cells: a six-transistor (6T) CMOS SRAM cell and a SRAM cell with transmission gates. And comparing them with respect to power in general, the cell design must strike a balance between cell area, robustness, speed, leakage and yield. Power reduction is one of the most important design objectives. However, the power cannot be reduced indefinitely without compromising the other parameters. For instance, low-power can compromise the cell area also speed of operation. The mainstream six-transistor (6T) CMOS SRAM cell is shown in figure -1, four transistors (q1−q4) comprise cross-coupled cmos inverters and two nmos transistors q5 and q6 provide read and write access to the cell. A 6T CMOS SRAM cell is the most popular sram cell due to its superior robustness, low power and low-voltage operation.

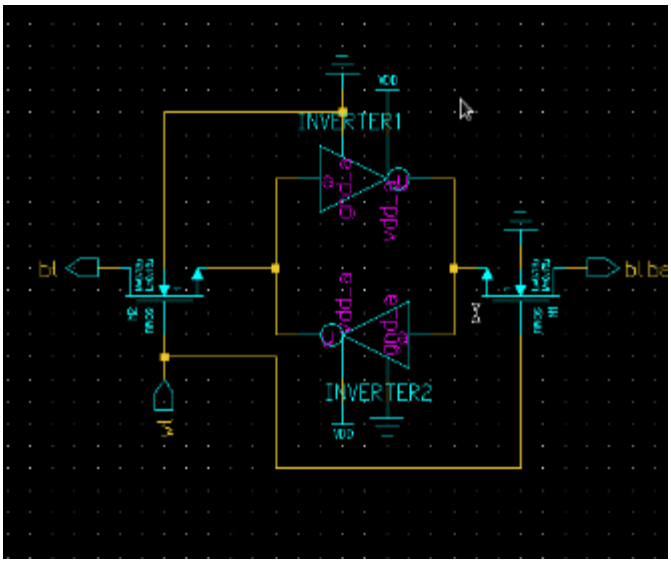

FIGURE 1: 6T SRAM CELL DESIGN

READ OPERATION

Read Operation Prior to initiating a read operation, the new read circuit is proposed as an individual read operation will be performed and the bit lines are precharged to VDD. The read operation is initiated by enabling the word line (WL) and connecting the precharged bit lines, BL and BLB, to the internal nodes of the cell. Upon read access, the bit line voltage VBL remains at the precharge level. The complementary bit line voltage VBLB is discharged through transistors Q1 and Q5 connected in series. Effectively, transistors Q1 and Q5 form a voltage divider whose output is now no longer at zero volt and is connected to the input of inverter Q2−Q4. Sizing of Q1 and Q5 should ensure that inverter Q2−Q4 do not switch causing a destructive read

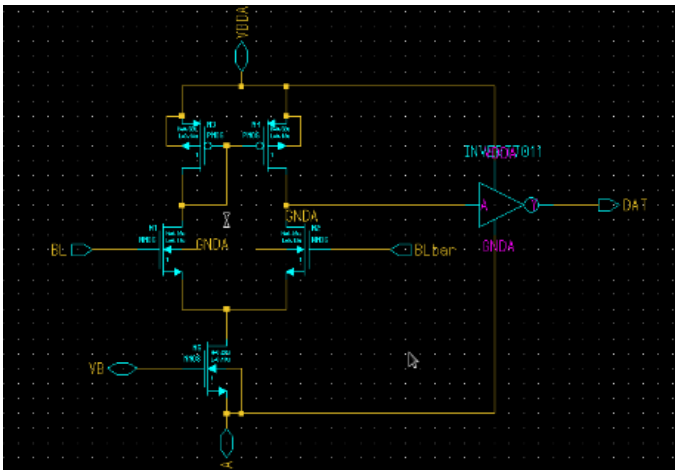

FIGURE :2 READ CIRCUIT OF A 6T SRAM CELL DESIGN

WRITE OPERATION:

For a standard write operation of a 6T SRAM cell neither performed using nor logic which it is performed, lowering one of the BITLINES to ground while asserting the WORDLINE does writing. To write a ’0’ BL is lowered, while writing a ’1’ requires BL to be lowered. Why is this? Let’s take a closer look at the cell when writing a ’1’ the cell has a ’0’ stored and for simplicity the schematic has been reduced in the same way as before. The main difference now is that the BITLINES no longer are released. Instead they are held at VCC and GND respectively. It can be seen from the left side of the memory cell (M1-M5) that it is virtually identical to the read operation. Since both BITLINES are now held at their respective value, the BITLINE capacitances have been omitted.

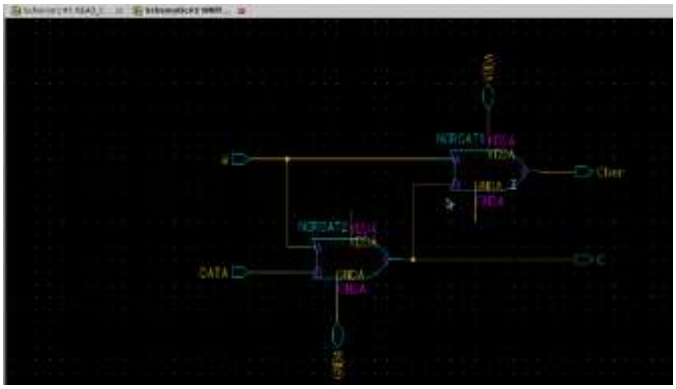

FIGURE 3: WRITE CIRCUIT OF A 6T SRAM CELL DESIGN

The write circuit is designed with the PMOS and NMOS transistor logic circuit and nor gate designed is used in this case and separate write and read circuit is designed and applied for the conventional SRAM cell for both write and read operation is observed and layout is designed for that circuit and implemented and its PEX and LVS results waves had been observed. In this write operation is based on BITLINE and BITLINE BAR with compared with WORDLINE and that will raise either from 0 to 1 or 1 to 0 for high reliable write operation.

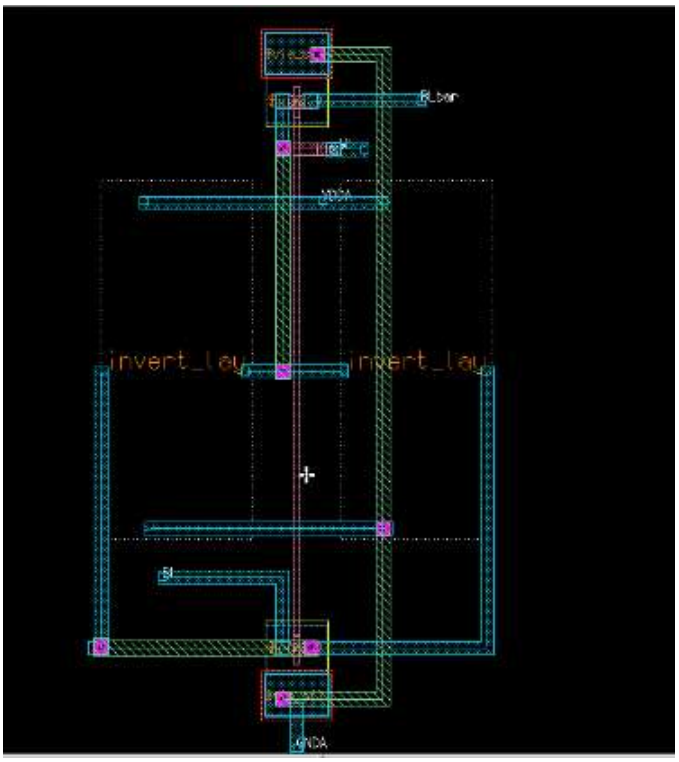

FIGURE 4: LAYOUT OF 6T SRAM CELL

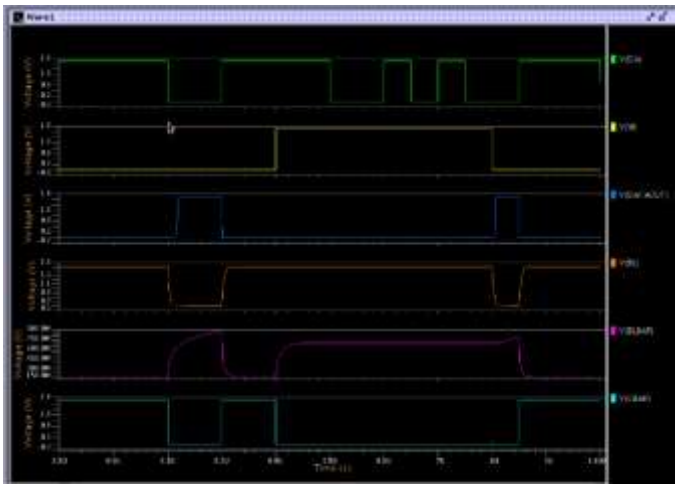

FIGURE 5: WITH PEX WAVEFORM OF A 6T SRAM CELL DESIGN

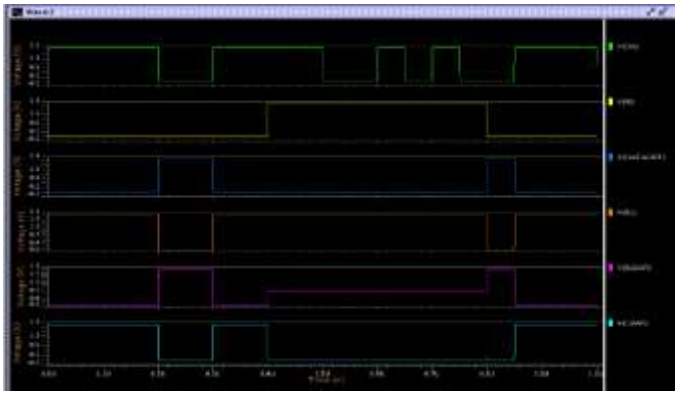

FIGURE 6: WITHOUT PEX WAVEFORM FOR 6T SRAM CELL

6T SRAM had been implemented and its write operation is observed with in decreasing the power supplies for BL and BLBAR. In the above circuit observing the conventional 6T SRAM by implementing this 6T SRAM circuit with a inverter using as a one input source for both BL and BLBAR and write operation is observed.

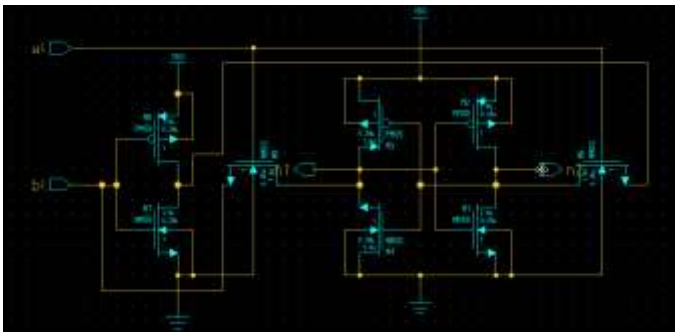

FIGURE 7:6T SRAM USING A INVERTER AS A POWER SOURCE

Schematic circuit for the above circuit is implemented by using a symbol with all the inputs and outputs in the above circuit and a pulse voltage is given to inputs and a dc voltage.

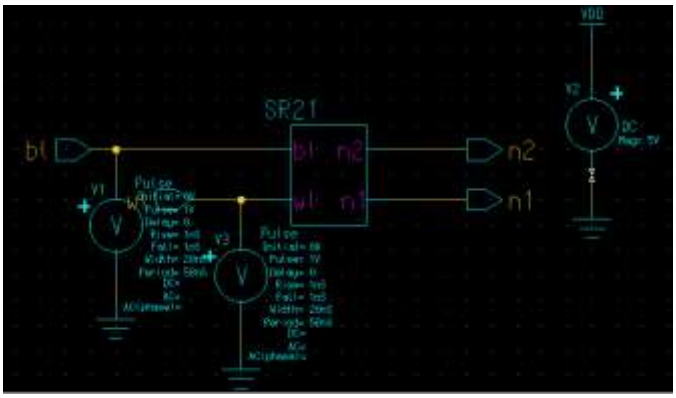

FIGURE 8: SCHEMATIC OF 6T SRAM CELL DESIGN

And its error report had checked after it had been verified for the results of dc analysis and trans analysis here the trans analysis had verified at different voltages from 0.5v to 2.5v with WL variation from 20ns to 60ns and from those result the perfect write operation is derived and observed that when we are applying the input voltage and the particular line voltage should be maintained for write operation.

Write operation will be observed with the terms of BL, BLBAR and WL when we are applying the input the BL and BLBAR will be in inverse and WL should raise either from 0 to 1 or from 1 to 0 and comparing the results of different voltages and particular write failure and correct write case had determined.

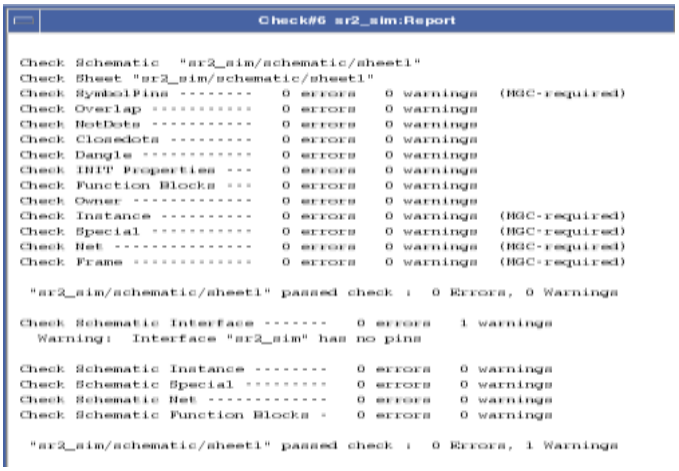

FIGURE 9: ERROR REPORT OF A SCHEMATIC 6T SRAM CELL

PROPOSED HIGH REALIABLE 6T SRAM CELL DESIGN

The proposed SRAM cell is shown in Figure, it consists of two transmission gates in place of pass (access) transistors as shown in Figure -1, this is due to the fact that the transmission gates have low voltage drop compare to pass transistors, also in the given cell we have an additional NMOS which acts as a switch and also it is necessary to restrict a short circuit current when the data is written in the elementary cell. However, the read and write operations of given circuit is same as that of conventional 6T CMOS SRAM cell.

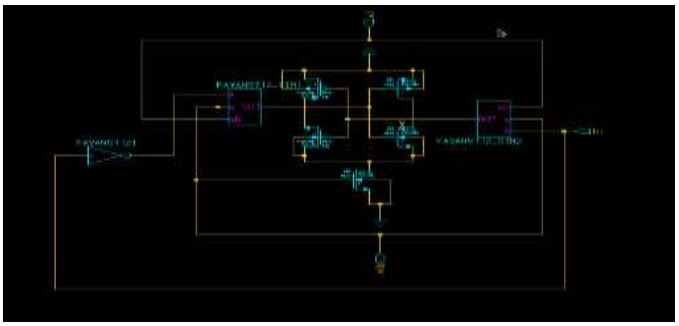

FIGURE 10: PROPOSED 6T SRAM WITH TRANSMISSION GATES

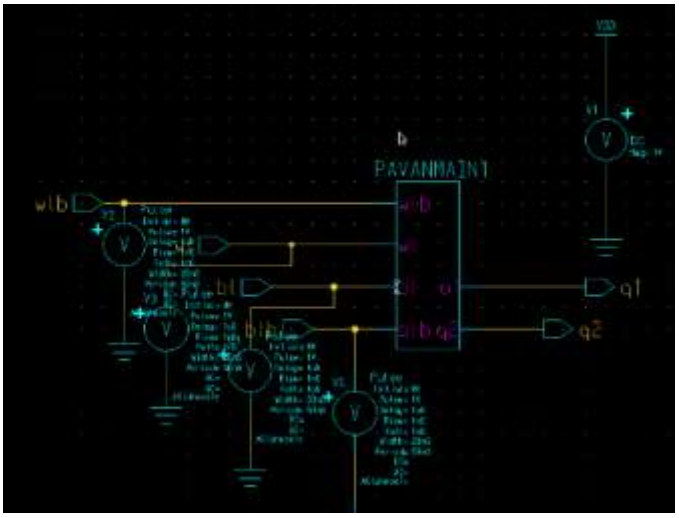

FIGURE 11: SCHEMATIC CIRCUIT FOR PROPOSED SRAM CELL

RESULTS

In this project studied and simulated both the circuits conventional SRAM cell as well as proposed SRAM cell as per the parameters shown in above and through simulation results shown that the write operation of proposed SRAM cell is much reliable than a conventional SRAM cell ,shown below is the comparison of write operation of both the circuits

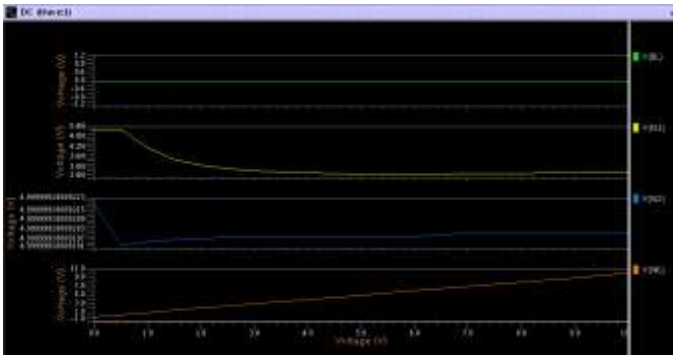

FIGURE 12: DC WAVEFORMS OF A 6T SRAM

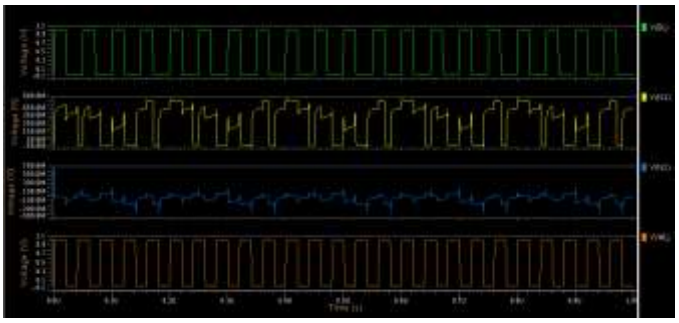

FIGURE 14: TRANS WAVEFORM AT 0.5V AND WL 20NS

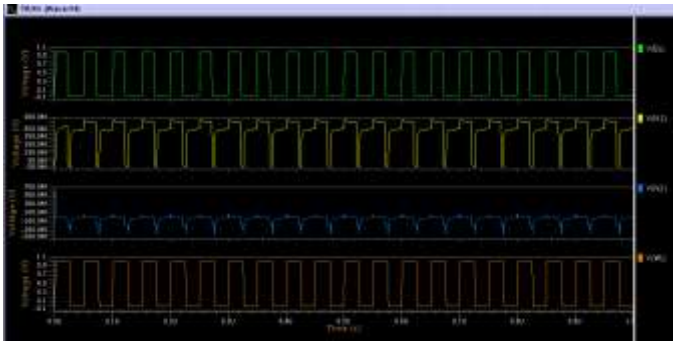

FIGURE 15: TRANS WAVEFORM AT 0.5V AND WL 25NS

FIGURE 16:TRAN WAVEFORM AY 1V AND WL60NS WRITE FAILURE CASE

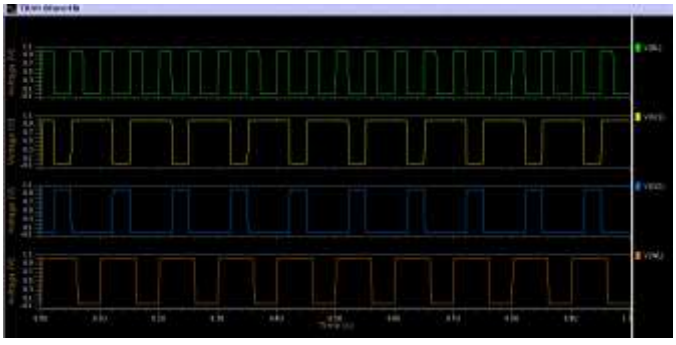

FIGURE 17: TRAN 1V AT WL 60NS(CORRECT WRITE OPERATION)

PROPOSED HIGH RELIABILITY ASSIST CIRCUITRY FOR SRAM

Proposed high reliability assist scheme is shown in fig below. As we know if more negative voltage peak is generated by negative bit line voltage, less will be reliability of the circuit. To overcome this problem, a capacitor is connected (whose other end is connected to ground) to the output of the NBLV generator which increases the absolute capacitance of the NBLV. This capacitor works as a low pass filter which smoothes out the negative voltage spike.

When level of negative voltage spike decreases, VGS of MOSFET reduces which reduces the strength of electric field. Due to low strength of electric field, these will be very low chances of dielectric breakdown and hence less chances of transistors'to get damaged, hence reliability of the circuit is increased.

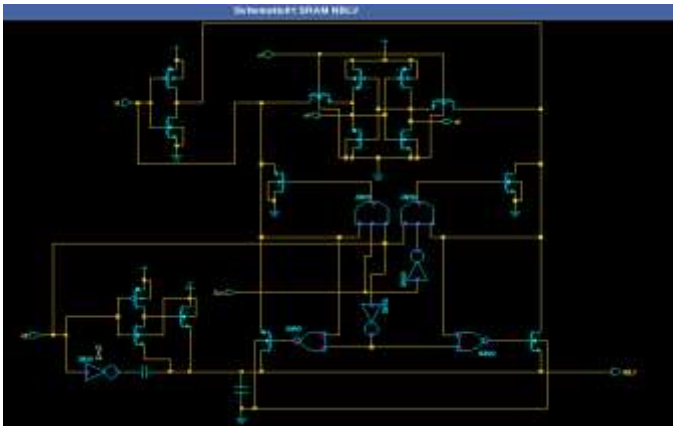

FIGURE 18: RELIABILITY ENHANCED WRITE ASSIST CIRCUIT

In this circuit we used a 6t SRAM cell which is used a sense amplifier and verified the write operation using NBLV technique. As we have seen that, to increase the reliability of the circuit, level of negative voltage generated by NBLV generator is reduced. But due to this reduced level of negative bit line voltage, the assisting effect of NBLV write assist scheme reduces which may cause the memory to fail. So, this reduced influence of assist circuit needs to be compensated to achieve high write ability and hence high efficiency of the SRAM. This compensation can be achieved by combining another write assist scheme with NBLV write assist scheme. So, we combine the word-line (WL) boost write assist scheme with NBLV write assist scheme. By combining these two schemes together we can achieve high reliability as well as write ability.

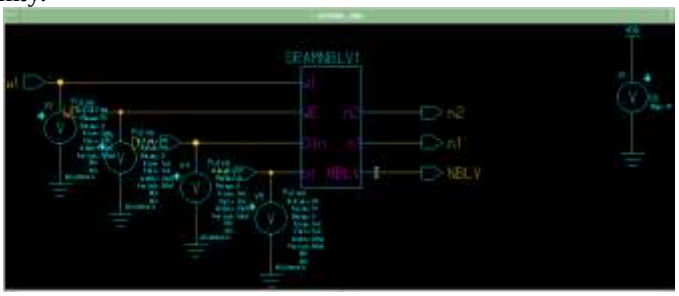

FIGURE 19: SCHEMATIC CIRCUIT OF NBLV

SIMULATION RESULTS

Schematic & simulation waveforms of high reliability negative bit-line write assist scheme is shown below in fig.(a) &(b). The proposed scheme is applied to SRAM and the waveforms are shown in fig.11 below. As we can see that nodes rb' and rt' are flipping successfully with a low level of negative bit line voltage as compared to voltage in conventional negative bit line voltage scheme. Because of this reduced level of negative bit line voltage, peak stress on transistors decreases and reliability of the circuit increases.

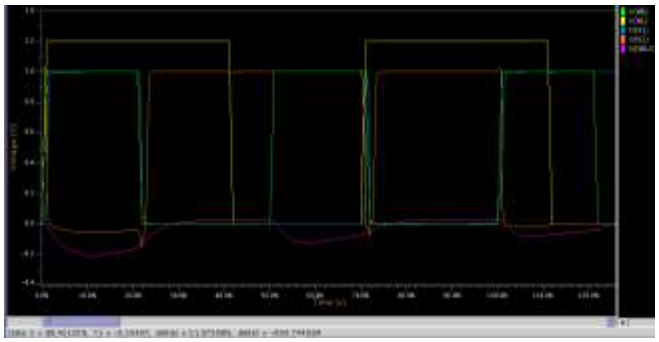

FIGURE 20: COMPARATIVE ANALYSIS OF NBLV

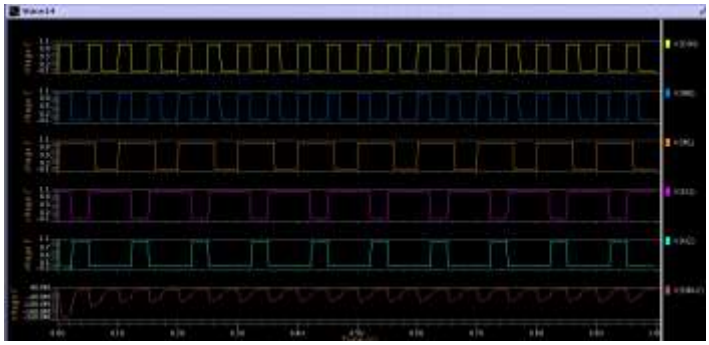

FIGURE 21:WRITE OPERATION WAVEFORM OF NBLV

CONCLUSION

In this paper, we have design and implemented a SRAM cell. And also analyzed the power consumption of conventional SRAM cell as well as proposed SRAM cell. The proposed SRAM cell has used two trapezoidal-wave pulses for controlled switching current flow. Observed that it is possible to reduce the power consumption and reliable write operation of CMOS SRAM cell by adding transmission gates as well as an NMOS switch to conventional CMOS 6T SRAM cell and NBLV implementation also observed.

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